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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WALLACE, SCOTT A	
ART UNIT	**PAPER NUMBER**
2675	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/502,994	MANTOR ET AL.	
	Examiner	Art Unit	
	Scott Wallace	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4-9,13,14 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4-9,13,14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 06/21/04 have been fully considered but they are not persuasive. As per applicant's argument that "Rivard fails to teach or suggest processing neighboring pixels of a primitive sequentially in accordance with a span based polygon rasterization scheme", Duluk (5,596,686) discloses using a span stepper for rasterization. Rivard does not disclose how the geometry gets rasterized but it is well known that the geometry has to get rasterized to be displayed on the monitor. Span based rasterization was a well known technique at the time of the invention therefore it was probably one of the techniques used. Also claim 18 does not disclose processing primitives sequentially, followed by the pixels by the next small spatial square.

2. As per applicant's argument that Gannett fails to teach a span based polygon rasterization scheme so neighboring pixels of a primitive will be processed sequentially. This is disclosed in Gannett in column 16 lines 47-65. "At each x,y pixel location along an edge of the triangle, the span stepper steps across the corresponding span". This means each pixel in processed in sequence.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rivard et al., U.S. Patent No. 6,300,953 in view of Duluk, Jr., U.S. Patent No. 5,596,686.

5. As per claim 18, Rivard et al discloses a method of controlling the transfer of texture data between a texture main memory and a texture cache memory (fig 2) while maintaining the most recently

used data in the texture cache memory comprising the steps of: a) receiving texture addresses for a first pixel, checking if the addresses match the addresses in a first stage of a multi-stage cache controller and doing one of the following, 1) loading the addresses in the first stage if there is no valid address in the first stage 2) reloading the addresses in the first stage if a match is found or 3) moving to a second stage if no match is found (column 6 lines 47-67 and fig 10);

b) if step a) 1) is true transferring the corresponding texture data from main memory into cache memory with a first tag (column 6 lines 47-67);

c) if step a) 2) is true, making no transfer of texture data because data has already been transferred (column 6 lines 47-67);

d) if step a) 3) is true, checking if the addresses match the addresses in the second stage and doing one of the following 1) if there is no addresses in the second stage moving the addresses from the first stage to the second stage and loading the addresses into the first stage 2) if a match is found moving the addresses from the first stage to the second stage and loading the addresses into the first stage 3) moving to a third stage if no match is found (column 6 lines 47-67);

e) if step d) 1) is true transferring corresponding texture data from the main memory into the cache memory with a second tag (column 6 lines 47-67);

f) if step d) 2) is true making no transfer of texture data because data has already been transferred(column 6 lines 47-67) ;

g) if step d) 3) is true, repeating step d) for subsequent stages and using subsequent tags where necessary, until a last stage been checked or until a match has been found (column 6 lines 47-67);

h) if the last stage has been checked and no match found loading the addresses into the first stage and moving the stored addresses to the next stage in sequence and overwriting the addresses from the last stage (column 6 lines 47-67) ;

i) if step h) is true transferring corresponding texture data from the main memory into cache memory with the tag of the last stage addresses (column 6 lines 47-67);

j) wherein when addresses are loaded into the first stage the tag assigned will be either the tag of the last stage or the tag within the stage that was hit (column 6 lines 47-67).

Also, Rivard et al does not disclose said cache controller transferring texture data at the main memory access granularity. This would have been obvious to one of ordinary skill in the art because to save time you would want the maximum number of bits of data being transferred, which is the granularity of the main memory. Also Rivard does not disclose wherein the method further includes processing neighboring pixels of a primitive sequentially in accordance with a span based polygon rasterization scheme. This is disclosed in Duluk in column 32 lines 30-60. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a span based rasterization because this was a well known technique to discard unwanted geometry before it gets rasterized. This would improve the processing speed since the unwanted stuff isn't rasterized.

6. Claims 2-9, 13, 14, 16-17, 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gannett, U.S. Patent No. 5,790,130.

7. As per claim 19, Gannett discloses a computer graphics processor system having the capability of mapping texture onto a three dimensional object in a scene being displayed (column 1 lines 45-50), the system comprising: a texture address calculator for generating texel address for a list of primitives being processed (column 1 lines 55-67); a texture main memory containing an array of texels, each texel having an address and one of N identifiers (fig 8 and column 19 lines 4-17 and column 22 lines 13-16); a texture cache memory having addresses partitioned into N banks (interleaves), each bank containing texels transferred from said main memory that have the corresponding identifier (column 18 lines 60-67 and column 22 lines 9-16); a texture cache controller for determining and requesting the necessary transfer of texels from said texture main memory addresses to said texture cache memory addresses (column 21 lines 55-64), said cache controller including a plurality of least recently used controllers coupled in

succession to thereby transfer texels according to a least recently used replacement algorithm, said texture cache controllers pre-fetching necessary neighboring texels from said texture main memory for bilinear filtering (column 9 lines 7-20 and column 22 lines 1-6); a texture cache arbiter (TIM) for scheduling and controlling the actual transfer of texels from said texture main memory into the texture cache memory (column 14 lines 25-45) and controlling the outputting of texels for each pixel to a interpolating filter from the cache memory (column 20 lines 60-67), wherein the method further includes processing neighboring pixels of a primitive sequentially in accordance with a span based polygon rasterization scheme (column 16 lines 45-65). Also, Gannett does not disclose said cache controller transferring texture data at the main memory access granularity. This would have been obvious to one of ordinary skill in the art because to save time you would want the maximum number of bits of data being transferred, which is the granularity of the main memory.

8. As per claim 14, Gannett discloses a computer graphics processor system having the capability of mapping texture onto a three dimensional object in a scene being displayed (column 1 lines 45-50), the system comprising: a texture address calculator for generating texel address for a list of primitives being processed (column 1 lines 55-67); a texture main memory containing an array of texels, each texel having an address and one of N identifiers (fig 8 and column 19 lines 4-17 and column 22 lines 13-16); a texture cache memory having addresses partitioned into N banks (interleaves), each bank containing texels transferred from said main memory that have the corresponding identifier (column 18 lines 60-67 and column 22 lines 9-16); a texture cache controller for determining and requesting the necessary transfer of texels from said texture main memory addresses to said texture cache memory addresses (column 21 lines 55-64); a texture cache arbiter (TIM) for scheduling and controlling the actual transfer of texels from said texture main memory into the texture cache memory (column 14 lines 25-45) and controlling the outputting of texels for each pixel to a interpolating filter from the cache memory (column 20 lines 60-67), said cache arbiter coupled for determining which texels in the cache memory can be overwritten when new texels are determined to be transferred to said cache memory by said cache controller (column 14

lines 25-45), said texture cache arbiter transfers said texels from said texture main memory into the cache memory according to a look-ahead algorithm to hide read and write access clock cycles between sequential pixels (column 22 lines 1-8, by reading texels from the cache as texels in parallel this hides read and write access because it skips them), wherein the method further includes processing neighboring pixels of a primitive sequentially in accordance with a span based polygon rasterization scheme (column 16 lines 45-65). However, Gannett does not specifically disclose that the cache arbiter (TIM) is coupled between said controller and said texture cache memory. It would have been obvious to one of ordinary skill in the art to couple the cache arbiter to the controller and cache memory because these are the components the arbiter manages therefore to have them in contact and close together would speed the transfer times between them. Also, Gannett does not disclose said cache controller transferring texture data at the main memory access granularity. This would have been obvious to one of ordinary skill in the art because to save time you would want the maximum number of bits of data being transferred, which is the granularity of the main memory.

9. As per claim 2, Gannett discloses wherein the system further includes a texture addressing scheme for organizing the array of texels in main memory to group spatially related texels in one memory page (column 17 lines 44-53).

10. As per claim 4, Gannett discloses wherein the texture mapping capability includes storing pre-filtered texture maps at different resolutions and bilinear interpolation texture filtering (column 2 lines 23-40 and column 20 lines 60-67).

Gannett discloses

11. As per claim 5, wherein said texture main memory contains an array of texels having addresses arranged in rows and columns, there being a plurality of even numbered rows and columns and a plurality of odd numbered rows and columns of texels, said texels having a per cache memory identifier attached to each address in accordance with the following criteria: a first identifier being assigned to texels that have addresses in both even rows and even columns of said memory; a seconf identifier being assigned to texels that have addresses in both even rows and odd columns of said main memory, a third identifier being assigned to texels that have addresses in both odd rows and even columns of said main memory,

and a fourth identifier being assigned to texels having addresses in both odd rows and odd columns of said main memory (column 22 lines 1-15 and fig 8).

12. As per claim 6, Gannett discloses wherein said texture cache memory is arranged in four banks (interleaves) of memory in accordance with the following criteria; a first bank (interleave) containing texels having the first identifier; a second bank (interleave) containing texels having the second identifier; a third bank (interleave) containing texels having the third identifier; and a fourth bank (interleave) containing texels having the fourth identifier (column 22 lines 1-15).

13. As per claim 7, Gannett discloses wherein N is equal to four (column 21 lines 55-64) and said texture main memory is organized into a plurality of texel blocks each having one of four block texel cache memory identifier (column 19 lines 4-20) in accordance with the following criteria: each texel block consisting of at least one group of four contiguous texels (column 22 lines 9-15), the texels in each group consisting of one of each of the per texel cache memory identifiers (column 22 lines 9-15), and wherein said texture cache memory being partitioned into a plurality of rows corresponding to said plurality of block texel cache memory identifiers (column 22 lines 9-15), each memory bank having at least one row corresponding to each of the four block texel cache memory identifiers (column 22 lines 9-15).

14. As per claim 8, Gannett discloses wherein the cache controller includes N stages (column 21 lines 55-64).

15. As per claim 9, Gannett discloses wherein cache controller includes N stages (column 21 lines 55-64).

16. As per claim 13, Gannett discloses wherein the texture cache memory is a multi-ported cache memory enabling multiple texel accesses per clock (column 21 lines 37-50).

17. As per claim 16, Gannett discloses wherein said texel blocks in said main memory each consist of a double quad word of data (column 21 lines 40-45, 4 double quad words).

18. As per claim 17, Gannett discloses wherein each row of said cache memory consisting of four sub-rows of data (interleaves A-D), each sub-row consisting of a pair of an even sub-row and an odd

sub-row (four adjacent texels), each double quad word being stored in one pair of said even and odd sub-row of said cache memory (column 21 lines 37-40 and column 22 lines 9-15).

Any response to this action should be mailed to:

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Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Wallace whose telephone number is 703-605-5163. The examiner can normally be reached on Monday thru Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz, can be reached on 703-306-0403. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sumati Lefkowitz

SUMATI LEFKOWITZ
PRIMARY EXAMINER